Ismail Emir Yuksel

PhD Student
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Research Interests

I am very passionate about designing efficient, robust, and secure computing systems. My research lies at the intersection of **computer architecture**, **memory-centric computing**, and **hardware security**, with a particular focus on understanding, enhancing, and exploiting fundamental computational capabilities and robustness of modern **DRAM** architectures.
My recent research projects focus on:

- Uncovering new *computational capabilities of real commodity DRAM chips* to enable low-cost memory-centric architectures.
- Understanding and exploring *read disturbance in DRAM* by rigorous characterization and analysis of real DRAM chips.
- Developing effective, high-performance, low-cost solutions that comprehensively *mitigate DRAM read disturbance*.

Education

ETH Zürich, Zürich, Switzerland — Feb. 2024 –
Ph.D., Computer Engineering (adviser: Onur Mutlu)

TOBB University of Economics and Technology, Ankara, Türkiye — 2019 – 2022
M.S. in Computer Engineering (adviser: Oğuz Ergin)
Thesis: "True Random Number Generation and Fault Modeling Methods for Reduced-Voltage SRAM Devices." (PDF)

TOBB University of Economics and Technology, Ankara, Türkiye — 2014 – 2019
B.S. in Electrical and Electronics Engineering (adviser: Oğuz Ergin)

Publications

Google scholar record: https://scholar.google.com/citations?user=qfK90PkAAAAJ&hl=en
DBLP record: https://dblp.org/pid/264/5883.html

First Author Publications & Preprints

1. Ismail Emir Yuksel, F. N. Bostanci, A. Olgun, O. Mutlu.
   "Memory-Centric Computing: Security Benefits and Challenges of Processing-in-DRAM'
   *Proceedings of the 38th ACM International Conference on Supercomputing (**ICS Workshops '26**)*, Jul. 2026.

2. Ismail Emir Yuksel, A. Olgun, F. N. Bostanci, O. Canpolat, G. F. Oliveira, M. Sadrosadati, A. G. Yaglikci, and O. Mutlu.
   "In-DRAM True Random Number Generation Using Simultaneous Multiple-Row Activation: An Experimental Study of Real DRAM Chips"
   *The 43rd IEEE International Conference on Computer Design (**ICCD**)*, Nov. 2025.

3. Ismail Emir Yuksel, A. Olgun, F. N. Bostanci, H. Luo, A. G. Yaglikci, O. Mutlu.
   "ColumnDisturb: Understanding Column-based Read Disturbance in Real DRAM Chips and Implications for Future Systems"
   *The 58th International Symposium on Microarchitecture (**MICRO**)*, Oct. 2025.
   One of the 12 computer architecture papers of 2025 selected as Top Picks by IEEE Micro.

4. Ismail Emir Yuksel, A. Sood, A. Olgun, O. Canpolat, H. Luo, F. N. Bostanci, M. Sadrosadati, A. G. Yaglikci, O. Mutlu.
   "PuDHammer: Experimental Analysis of Read Disturbance Effects of Processing-using-DRAM in Real DRAM Chips"
   *The 52nd International Symposium on Computer Architecture (**ISCA**)*, Jun. 2025.

5. Ismail Emir Yuksel, Y. C. Tugrul, F. N. Bostanci, G. F. Oliveira, A. G. Yaglikci, A. Olgun, M. Soysal, H. Luo, J. Gomez-Luna, M. Sadrosadati, O. Mutlu.
   "Simultaneous Many-Row Activation in Off-the-Shelf DRAM Chips: Experimental Characterization and Analysis."
   *The 54th International Conference on Dependable Systems and Networks (**DSN**)*, Jun. 2024.
   Open source code: https://github.com/CMU-SAFARI/SiMRA-DRAM
   Officially artifact evaluated as available, reusable and reproducible.

6. Ismail Emir Yuksel, Y. C. Tugrul, A. Olgun, F. N. Bostanci, A. G. Yaglikci, G. F. Oliveira, H. Luo, J. Gomez-Luna, M. Sadrosadati, O. Mutlu.
   "Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis."
   *The 30th International Symposium on High-Performance Computer Architecture (**HPCA**)*, Apr. 2024.
   Open source code: https://github.com/CMU-SAFARI/FCDRAM

7. Ismail Emir Yuksel, A. Olgun, B. Salami, F. N. Bostanci, Y. C. Tugrul, A. G. Yaglikci, N. M. Ghiasi, O. Mutlu, O. Ergin.
   "TuRaN: True Random Number Generation Using Supply Voltage Underscaling in SRAMs."
   arXiv, Nov. 2022.

8. Ismail Emir Yuksel, B. Salami, O. Ergin, O. S. Unsal, A. Cristal.
"MoRS: An Approximate Fault Modeling Framework for Reduced-Voltage SRAMs"
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, Oct. 2021.

Other Publications

9. A. Olgun, H. Luo, Ismail Emir Yuksel, F. N. Bostanci, A. G. Yaglikci, M. Sadrosadati, O. Mutlu.
"A Modern Large-Scale Memory Characterization Laboratory'
*Proceedings of the 38th ACM International Conference on Supercomputing (**ICS Workshops '26**)*, Jul. 2026.

10. D. Tokuda, T. Kubo, Ismail Emir Yuksel, A. Olgun, H. Luo, T. Nagatani, G. F. Oliveira, A. G. Yaglikci, M. Sadrosadati, O. Mutlu, S. Takamaeda-Yamazaki.
"Clutch: High Performance Vector-Scalar Comparison using DRAM via Chunked Temporal Coding"
*Proceedings of the 38th ACM International Conference on Supercomputing (**ICS**)*, Jul. 2026.

11. R. Nadig, V. Arulchelvan, R. Bera, T. Shahroodi, G. Singh, A. Kakolyris, Ismail Emir Yuksel, M. Sadrosadati, J. Park, O. Mutlu.
"Harmonia: Enhancing Data Placement and Migration in Hybrid Storage Systems via Multi-Agent Reinforcement Learning"
*Proceedings of the 38th ACM International Conference on Supercomputing (**ICS**)*, Jul. 2026.

12. H. Luo, Ismail Emir Yuksel, A. Olgun, F. N. Bostanci, O. Ecemis, A. G. Yaglikci, O. Mutlu.
"DejaVu: Why You Should Write to Your DRAM Rows Twice"
*The 53rd International Symposium on Computer Architecture (**ISCA**)*, Jun. 2026.

13. D. Tokuda, Ismail Emir Yuksel, T. Kubo, A. Olgun, H. Luo, F. N. Bostanci, J. Wang, A. G. Yaglikci, S. Takamaeda-Yamazaki, O. Mutlu.
"Altering Processing-using-DRAM Operation Results Without Changing Operands: A Study of Real DRAM Chips and Implications for Future Systems"
*The 53rd International Symposium on Computer Architecture (**ISCA**)*, Jun. 2026.

14. A. K. Kakolyris, F. N. Bostanci, A. Olgun, Ismail Emir Yuksel, K. M. Sgouras,H. Songara, K. Kanellopoulos, U. Baser, A. G. Yaglikci, O. Mutlu.
"ColumnKeeper: Efficient Solutions for Mitigating ColumnDisturb in DRAM-based Systems"
*The 53rd International Symposium on Computer Architecture (**ISCA**)*, Jun. 2026.

15. J. Wang, H. Luo, A. Olgun, Ismail Emir Yuksel, A. G. Yaglikci, Y. Liang, F. N. Bostanci, M. Sadrosadati, O. Mutlu
"ScaleHammer: Exploiting Temporal Asymmetry to Amplify Read Disturbance in Modern DRAM Chips"
*The 56th International Conference on Dependable Systems and Networks (**DSN**), Jun. 2026.*

16. U. Baser, Ismail Emir Yuksel, F. N. Bostanci, K. Sgouras, A. Olgun, E. H. Demirli, Z. Yue, H. Songara, O. Ergin, O. Mutlu.
"In-DRAM Signature Generation Using Simultaneous Multiple-Row Activation: An Experimental Study of Off-The-Shelf DRAM Chips."
*The 56th International Conference on Dependable Systems and Networks Disrupt Track (**DSN Disrupt**)*, Jun. 2026.

17. F. N. Bostanci, O. Canpolat, A. Olgun, Ismail Emir Yuksel, K. Kanellopoulos, M. Sadrosadati, A. G. Yaglikci, O. Mutlu.
"Understanding and Mitigating Covert and Side Channel Vulnerabilities Introduced by RowHammer Defenses"
*The 58th International Symposium on Microarchitecture (**MICRO**)*, Oct. 2025.
Officially artifact evaluated as available, functional, and reproduced.

18. F. N. Bostanci, K. Kanellopoulos, A. Olgun, A. G. Yaglikci, Ismail Emir Yuksel, N. M. Ghiasi, Z. Bingol, M. Sadrosadati, O. Mutlu.
"Revisiting Main Memory-Based Covert and Side Channel Attacks in the Context of Processing-in-Memory"
*The 55th International Conference on Dependable Systems and Networks (**DSN**), Jun. 2025.*
Open source code: https://zenodo.org/records/15116851
Officially artifact evaluated as available, reviewed, and reproduced.

19. O. Mutlu, A. Olgun, Ismail Emir Yuksel.
"Memory-Centric Computing: Solving Computing's Memory Problem"
*Invited Paper in Proceedings of the 17th IEEE International Memory Workshop (**IMW**), May 2025.*

20. H. Luo, Ismail Emir Yuksel, A. Olgun, A. G. Yaglikci, O. Mutlu.
"Revisiting DRAM Read Disturbance: Identifying Inconsistencies Between Experimental Characterization and Device-Level Studies"
*To appear in the 43rd IEEE VLSI Test Symposium (**VTS**), Apr. 2025.*

21. O. Canpolat, A. G. Yaglikci, G. F. Oliveira, A. Olgun, F. N. Bostanci, Ismail Emir Yuksel, H. Luo, O. Ergin, O. Mutlu.
"Chronus: Understanding and Securing the Cutting-Edge Industry Solutions to DRAM Read Disturbance."
*The 31st International Symposium on High-Performance Computer Architecture (**HPCA**)*, Mar. 2025.

Open source code: https://github.com/CMU-SAFARI/Chronus
Officially artifact evaluated as available, reusable and reproducible.

22. Y. Tugrul, A. G. Yaglikci, Ismail Emir Yuksel, A. Olgun, O. Canpolat, F. N. Bostanci, M. Sadrosadati, O. Ergin, O. Mutlu.
"Understanding RowHammer Under Reduced Refresh Latency: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions."
*The 31st International Symposium on High-Performance Computer Architecture (**HPCA**)*, Mar. 2025.
Open source code: https://github.com/CMU-SAFARI/PaCRAM
Officially artifact evaluated as available, reusable and reproducible.
Distinguished artifact award at HPCA 2025.

23. A. Olgun, N. Bostanci, Ismail Emir Yuksel, A. G. Yaglikci, G. F. Oliveira, H. Luo, O. Canpolat, M. Patel, O. Mutlu.
"Variable Read Disturbance: An Experimental Analysis of Temporal Variation in DRAM Read Disturbance."
*The 31st International Symposium on High-Performance Computer Architecture (**HPCA**)*, Mar. 2025.

24. O. Mutlu, A. Olgun, G. F. Oliveira, Ismail Emir Yuksel.
"Memory-Centric Computing: Recent Advances in Processing-in-DRAM."
*Invited Paper in Proceedings of the 70th Annual IEEE International Electron Devices Meeting (**IEDM**), Dec. 2024.*

25. O. Canpolat, A. G. Yaglikci, A. Olgun, Ismail Emir Yuksel, Y.C. Tugrul, K. Kanellopoulos, O. Ergin, and O. Mutlu.
"BreakHammer: Enhancing RowHammer Mitigations by Carefully Throttling Suspect Threads."
*The 57th International Symposium on Microarchitecture (**MICRO**)*, Nov. 2024.
Open source code: https://github.com/CMU-SAFARI/BreakHammer
Officially artifact evaluated as available, reusable and reproducible.

26. A. Olgun, Y. C. Tugrul, N. Bostanci, Ismail Emir Yuksel, H. Luo, S. Rhyner, A. G. Yaglikci, G. F. Oliveira, O. Mutlu.
"ABACuS: All-Bank Activation Counters for Scalable and Low Overhead RowHammer Mitigation."
*The 33rd USENIX Security Symposium (**USENIX Security**)*, Aug. 2024.
Open source code: https://github.com/CMU-SAFARI/ABACuS
Officially artifact evaluated as available, functional, and reproduced.

27. H. Luo, Ismail Emir Yuksel, A. Olgun, A. G. Yaglikci, M. Sadrosadati, O. Mutlu.
"An Experimental Characterization of Combined RowHammer and RowPress Read Disturbance in Modern DRAM Chips."
*The 54th International Conference on Dependable Systems and Networks Disrupt Track (**DSN Disrupt**)*, Jun. 2024.

28. A. G. Yaglikci, G. F. Oliveira, Y. C. Tugrul, Ismail Emir Yuksel, A. Olgun, H. Luo, O. Mutlu.
"Spatial Variation-Aware Read Disturbance Defenses: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions."
*The 30th International Symposium on High-Performance Computer Architecture (**HPCA**)*, Apr. 2024.

29. F. N. Bostanci, Ismail Emir Yuksel, A. Olgun, K. Kanellopoulos, Y. C. Tugrul, A. G. Yaglikci, M. Sadrosadati, O. Mutlu.
"CoMeT: Count-Min-Sketch-based Row Tracking to Mitigate RowHammer at Low Cost."
*The 30th International Symposium on High-Performance Computer Architecture (**HPCA**)*, Apr. 2024.
Open source code: https://github.com/CMU-SAFARI/CoMeT
Officially artifact evaluated as available, reusable and reproducible.

30. E. B. Onural, Ismail Emir Yuksel, B. Salami.
"Demonstrating Reduced-Voltage FPGA-based Neural Network Acceleration for Power-Efficiency"
*The 30th International Conference on Field-Programmable Logic and Applications (**FPL**)*, Aug. 2020.

31. B. Salami, E. B. Onural, Ismail Emir Yuksel, F. Koc, O. Ergin, A. C. Kestelman, O. Unsal, H. Sarbazi-Azad, O. Mutlu.
"An Experimental Study of Reduced-Voltage Operation in Modern FPGAs for Neural Network Acceleration"
*The 50th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (**DSN**)*, Jun. 2020.

Invited Talks, Lectures, Tutorials

1. "Understanding Read Disturbance in Real DRAM Chips: What Comes After RowHammer and RowPress"
   - University of New South Wales, Sydney, Australia, 6 February 2026.
2. "Understanding the Computational Capabilities of Real DRAM Chips and Robustness Issues They Introduce"
   - University of Sydney, Sydney, Australia, 5 February 2026.
   - University of Tokyo, Tokyo, Japan, 31 October 2025.
   - Ritsumeikan University, Osaka, Japan, 30 October 2025.
   - KAIST, Daejeon, South Korea, 23 October 2025.
3. "Processing-using-Memory in Real DRAM Chips"
   - The 4th Workshop on Memory-Centric Computing Systems at HPCA'26, Sydney, Australia, 1 February 2026.
   - The 5th Workshop on Memory-Centric Computing Systems at ASPLOS'26, Pittsburgh, USA, 23 March 2026.
4. "Understanding the Computational Capabilities of COTS DRAM Chips"

- The 1st SAFARI Live Workshop (SaLWo) on Data-Centric and Energy-Efficient Computing, Zurich, 21 July 2025.

5. "PuDHammer: Experimental Analysis of Read Disturbance Effects of Processing-using-DRAM in Real DRAM Chips"
   - The 1st SAFARI Live Workshop (SaLWo) on Memory Robustness, Zurich, 10 July 2025.
   - The 3rd Workshop on Memory-Centric Computing Systems at ISCA'25, Tokyo, Japan, 21 June 2025.
6. "Functionally-Complete Boolean Logic in Real DRAM Chips"
   - The 2nd Workshop on Memory-Centric Computing Systems at ICS'25, Salt Lake City, USA, 8 June 2025.

Conference Talks

7. "In-DRAM True Random Number Generation Using Simultaneous Multiple-Row Activation: An Experimental Study of Real DRAM Chips."
   *The 43rd IEEE International Conference on Computer Design (**ICCD**)*, Dallas, TX, USA, November 2025.
8. "ColumnDisturb: Understanding Column-based Read Disturbance in Real DRAM Chips and Implications for Future Systems."
   *The 58th International Symposium on Microarchitecture (**MICRO**)*, Seoul, South Korea, October 2025.
9. "PuDHammer: Experimental Analysis of Read Disturbance Effects of Processing-using-DRAM in Real DRAM Chips."
   *The 52nd International Symposium on Computer Architecture (**ISCA**)*, Tokyo, Japan, June 2025.
10. "Simultaneous Many-Row Activation in Off-the-Shelf DRAM Chips: Experimental Characterization and Analysis."
    The 54th Annual International Conference on Dependable Systems and Networks (**DSN**), Brisbane, Australia, June 2024.
11. "Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis."
    *The 30th International Symposium on High-Performance Computer Architecture (**HPCA**)*, Edinburgh, Scotland, March 2024.

Workshops

1. **"The Seventh Workshop on Memory-Centric Computing (MCCSys) at ICS'26"**
   https://events.safari.ethz.ch/ics-MCCSys/
   Lead Organizer, Belfast, Northern Ireland, UK, July 2026
2. **"The Third Tutorial on Ramulator & DRAM Bender: Cutting-Edge Infrastructures for Real and Future Memory System Evaluation at ICS'26"**
   https://events.safari.ethz.ch/isca26-ramulator-drambender/
   Organizer, Belfast, Northern Ireland, UK, July 2026
3. **"The Sixth Workshop on Memory-Centric Computing (MCCSys) at ISCA'26"**
   https://events.safari.ethz.ch/isca-MCCSys/
   Lead Organizer, Raleigh, USA, June 2026
4. **"The Second Tutorial on Ramulator & DRAM Bender: Cutting-Edge Infrastructures for Real and Future Memory System Evaluation at ISCA'26"**
   https://events.safari.ethz.ch/isca26-ramulator-drambender/
   Organizer, Raleigh, USA, June 2026
5. **"The First Tutorial on Ramulator & DRAM Bender: Cutting-Edge Infrastructures for Real and Future Memory System Evaluation at ASPLOS'26"**
   https://events.safari.ethz.ch/asplos26-ramulator-drambender/
   Organizer, Pittsburgh, USA, March 2026
6. **"The Fifth Workshop on Memory-Centric Computing (MCCSys) at ASPLOS'26"**
   https://events.safari.ethz.ch/asplos26-MCCSys/
   Lead Organizer, Pittsburgh, USA, March 2026
7. **"The Fourth Workshop on Memory-Centric Computing (MCCSys) at HPCA'26"**
   https://events.safari.ethz.ch/hpca26-MCCSys/
   Lead Organizer, Sydney, Australia, February 2026

Teaching Experience

- **FPGA-based Exploration of DRAM and RowHammer** (BS Level), ETH Zürich, *Lecturer* 2023-2024
- **Digital Design and Computer Architecture** (BS Level), ETH Zürich, *Teaching Assistant* 2023-2025
- **Computer Architecture** (MS Level), ETH Zürich, *Teaching Assistant* 2023-2025
- **Seminar in Computer Architecture** (BS Level), ETH Zürich, *Teaching Assistant* 2023-2025
- **Computer Architecture and Organization** (BS Level), TOBB ETÜ, *Teaching Assistant* 2019-2022
- **Digital Design** (BS Level), TOBB ETÜ, *Teaching Assistant and Lecturer* 2019-2022

Student Mentorship

- **ETH Zürich Undergraduate Students**: Fabian Repplinger (2023-2024), Maria Maakenkova (2023-2024), Cristina Morad (2024)
- **ETH Zürich Graduate Students**: Akash Sood (2024-2025), Fabian Repplinger (2025-), Konstantinos Sgouras (2025-), Harsh Songara (2026-)
- **Other Students**: Daichi Tokuda (MS, University of Tokyo, 2025-), Umut Baser (MS, TOBB ETU, 2025-), Ipek Akdeniz (MS, TUM, 2025-), Orhun Ecemis (BS, TOBB ETU, 2025-)

Service

- *Technical reviewer for Journals:* IEEE TETC, IEEE CAL
- *Technical Subreviewer for Conferences:* ISCA, MICRO, HPCA, DSN, ASPLOS, ICS
- *Technical Subreviewer for Journals:* IEEE MICRO Top Picks, ACM TECS, Microelectronics Reliability, IEEE TCAD
- *FPGA-based DRAM Testing Infrastructure Lead*, SAFARI Research Group, ETH Zürich, 2024-